225, filter 214, and related aspects of processing system 200 can comprise means for estimating a voltage deviation that will occur if a transaction is executed in a pipeline of the processing system. Threshold comparators 216 and 218 can comprise means for determining if the estimated voltage deviation exceeds a specified threshold. In exemplary aspects, scheduler 206 (comprising issue queue 207) can also comprise means for implementing one or more corrective measures to mitigate voltage deviation, before the transaction is issued to be executed in the pipeline if the estimated voltage deviation exceeds a specified threshold.

[0059] In FIG. 4, a block diagram of a particular illustrative aspect of computing device 400 according to exemplary aspects is illustrated. Computing device 400 may be configured to perform method 300 of FIG. 3 in some aspects. Computing device 400 includes system-in-package or system-on-chip device 422 which may be similar to processing system 200 of FIG. 2. Only selected aspects of processing system 200 from FIG. 2 are shown in the representation of computing device 400 in FIG. 4, while other features have been omitted for the sake of clarity. As shown, computing device 400 includes processor 402 which is shown to comprise scheduler 206, energy table 225, filter 214, and pipeline 210 of FIG. 2 (the connection between energy table 225 and scheduler 206 is shown in dashed lines to convey that information from energy table 225 may be used to derive incoming energy 228 which is supplied to scheduler 206 as explained with reference to FIG. 2). It will be noted that the various other functional blocks of processing system 200 and related interconnections, although not illustrated herein, may be implemented in computing device 400. As shown in FIG. 4, processor 402 may be in communication with memory 432. Although not shown, one or more caches (e.g., I-cache 202) or other memory structures may also be included in computing device 400.

[0060] FIG. 4 also shows display controller 426 that is coupled to processor 402 and to display 428. Coder/decoder (CODEC) 434 (e.g., an audio and/or voice CODEC) can be coupled to processor 402. Other components, such as wireless controller 440 (which may include a modem) are also illustrated. Speaker 436 and microphone 438 can be coupled to CODEC 434. FIG. 4 also indicates that wireless controller 440 can be coupled to wireless antenna 442. In a particular aspect, processor 402, display controller 426, memory 432, CODEC 434, and wireless controller 440 are included in the aforementioned system-in-package or system-on-chip device 422.

[0061] In a particular aspect, input device 430 and power supply 444 are coupled to the system-on-chip device 422. Moreover, in a particular aspect, as illustrated in FIG. 4, display 428, input device 430, speaker 436, microphone 438, wireless antenna 442, and power supply 444 are external to the system-on-chip device 422. However, each of display 428, input device 430, speaker 436, microphone 438, wireless antenna 442, and power supply 444 can be coupled to a component of the system-on-chip device 422, such as an interface or a controller.

[0062] It should be noted that although FIG. 4 depicts a wireless communications device, processor 402 and memory 432 may also be integrated into a set-top box, a music player, a video player, an entertainment unit, a navigation device, a personal digital assistant (PDA), a fixed location data unit, or a computer. Further, at least one or more exemplary aspects of computing device 400 may be integrated in at least one semiconductor die.

[0063] Those of skill in the art will appreciate that information and signals may be represented using any of a variety of different technologies and techniques. For example, data, instructions, commands, information, signals, bits, symbols, and chips that may be referenced throughout the above description may be represented by voltages, currents, electromagnetic waves, magnetic fields or particles, optical fields or particles, or any combination thereof.

[0064] Further, those of skill in the art will appreciate that the various illustrative logical blocks, modules, circuits, and algorithm steps described in connection with the aspects disclosed herein may be implemented as electronic hardware, computer software, or combinations of both. To clearly illustrate this interchangeability of hardware and software, various illustrative components, blocks, modules, circuits, and steps have been described above generally in terms of their functionality. Whether such functionality is implemented as hardware or software depends upon the particular application and design constraints imposed on the overall system. Skilled artisans may implement the described functionality in varying ways for each particular application, but such implementation decisions should not be interpreted as causing a departure from the scope of the present invention.

[0065] The methods, sequences and/or algorithms described in connection with the aspects disclosed herein may be embodied directly in hardware, in a software module executed by a processor, or in a combination of the two. A software module may reside in RAM memory, flash memory, ROM memory, EPROM memory, EEPROM memory, registers, hard disk, a removable disk, a CD-ROM, or any other form of storage medium known in the art. An exemplary storage medium is coupled to the processor such that the processor can read information from, and write information to, the storage medium. In the alternative, the storage medium may be integral to the processor.

[0066] Accordingly, an aspect of the invention can include a computer readable media embodying a method of operating a processor, and more specifically, controlling voltage deviations in the processor. Accordingly, the invention is not limited to illustrated examples and any means for performing the functionality described herein are included in aspects of the invention.

[0067] While the foregoing disclosure shows illustrative aspects of the invention, it should be noted that various changes and modifications could be made herein without departing from the scope of the invention as defined by the appended claims. The functions, steps and/or actions of the method claims in accordance with the aspects of the invention described herein need not be performed in any particular order. Furthermore, although elements of the invention may be described or claimed in the singular, the plural is contemplated unless limitation to the singular is explicitly stated.

1. A method of controlling voltage deviation in a processing system, the method comprising:

estimating a voltage deviation that will occur if a transaction is executed in a pipeline of the processing system;

determining if the estimated voltage deviation exceeds a specified threshold; and